

XRTC 2018 Agenda (by Session)

S Special			
S-1	Welcome and Introductions	Caroline Ryan Wu, Xilinx A & D	5
S-2	Annual Meeting Overview	Gary Swift, Swift ERS	20
S-3	Presentation Introductions	Jim Devereaux, Xilinx FAE	5
S-4	Keynote Address		
	Insights into Three(-plus) Decades of FPGAs	Steve Trimberger, self (Xilinx retired)	60
A Test Results			
A1	V7 : Overview & LET Assignments	Gary Swift, Swift ERS	20
A2	US : NEPP Results, Mishaps, & Plans	Melanie Berg, (NASA/GSFC)	20
A3	V7 : Clocking Resources	Kevin Wray, Boeing	20
A4	US+ & US : Proton Upset Results	Valeri Kirischian, MDA/Maxan	20
A5	V7 : BRAMs & BRAM ECC	Bill Rowe, Raytheon	20
A6	V7 : BRAMs & Config MCUs	Prof. Mike Wirthlin, BYU	20
A7	US+ : Config, BRAM, & Flip-Flops	David Lee, Sandia	20
A8	V7 : IOBs	Sebastian Garcia, S-Labs	20
A9	V7 : IOSERDES	Krystin Pfau, Raytheon	10
A10	V7 : SEFIs	Gary Swift, Swift ERS	10
NDA	US : TID Results	Pierre Maillard, Xilinx Technology Development	30*
B Projects and Missions			
B1	Methods for Permanent Fault Handling in FPGAs	Florian Rittner, Friedrich-Alexander-Universität	20
B2	Los Alamos FPGAs-in-Space Experience	Heather Quinn, LANL	20
B3	Framework for On-orbit Reconfiguration	Christopher Stender, Fraunhofer IIS	30
B4	tba		20
C Test Infrastructure: Hardware and Boards			
C1	Overview: XRTC Gen4 CTI Apparatus	Gary Swift, Swift ERS	20
C2	Using COTS Test Apparatus	Joe Marshall, BAE	20
C3	Details: Gen4 Test Boards	Gary Swift, Swift ERS	20
C4	XRTC Common Test Infrastructure Boards	Neil Sampson, STS	30
C5	Details: BrainBox Operation	Gary Swift, Swift ERS	30
C6	Details: SMAP JCM Capabilities & Tools	Prof. Mike Wirthlin, BYU	20
C7	Looking Ahead: Gen4 Improvements	Gary Swift, Swift ERS	20
C8	Status: FMC-based, Motherboard-less Concept	David Lee, Sandia	10
D Test Planning			
D1	KU060 Campaign Overview	Gary Swift, Swift ERS	20
D2	SEL Suppression w/ US+	Eliot Glaser, NGC	20
D3	Misc'l: V7 Primitives, Processors, Mitigation	Gary Swift, Swift ERS	20
D4	Flight Designs : In-Beam Test Capability	Gary Swift, Swift ERS	20
E Ecosystem			
E1	Space Eval KU060 Platform	Adam Smith, Alpha-Data	20
E2	Exhaustive Formal Verification: EDACed State	Mark Eslingler, Mentor Graphics	20
E3	RapidIO IP for Space FPGAs	Kent Dahlgren, Praesum Communications	20
E4	KU060 & V5 Adjunct Space Parts/Solutions	Javier Valle, Texas Instruments	20
E5	Memory Infrastructure for Space FPGAs	Helmut Puchner, Cypress	20

T Topics of Interest			
T1	FPGAs-in-Space: Infrequently Asked Questions	Eric Crabill, Xilinx TM for SEUs	30
T2	TMR: Removing Common Mode Fail Points	Prof. Mike Wirthlin, BYU	20
T3	Terrestrial Upsets, Rosetta, and FPGA Scaling	Austin Lesea, Swift ERS	20
T4	Test H/W sans RTL: Pynq Board Overview	Patrick Lysaght, Xilinx	30
T5	Vivado Tutorial & Demo	Jim Devereaux, Xilinx FAE	40
T6	Fitting Thinned Die via Kriging	Sebastian Garcia, S-Labs	20
F Infrastructure: Software, IP, & Methodology			
F1	Overview: XRTC Test Methodologies	Gary Swift, Swift ERS	20
F2	Mitigation Testing – Tri-flux Methodology	Gary Swift, Swift ERS	20
F3	GUIs: FuncMon, ConfigMon, & FaultMon	Gary Swift, Swift ERS	20
F4	TURTLE Fault Injection Infrastructure & Results	Prof. Mike Wirthlin, BYU	20
F5	Using Python for XRTC Data Analysis	Gary Swift, Swift ERS	20